

CLAIMS:

1. A digital signal processing apparatus for executing a plurality of operations, comprising

a plurality of functional units (10) wherein each functional unit (10) is adapted to execute operations, and

5 control means for controlling said functional units (10), characterized in that said control means comprises a plurality of control units (12) wherein at least one control unit (12) is operatively associated to any functional unit (10), respectively, for controlling its function, and each functional unit (10) is adapted to execute operations in an autonomous manner under control by the control unit (12) associated thereto.

10 2. Apparatus according to claim 1, characterized by FIFO (first-in/first-out) register means (14) adapted for supporting data-flow communication among said functional units (10).

15 3. A digital signal processing apparatus for executing a plurality of operations, comprising a plurality of functional units (10) wherein each functional unit (10) is adapted to execute operations, and

20 control means for controlling said functional units (10), characterized by FIFO (first-in/first-out) register means (14) adapted for supporting data-flow communication among said functional units (10).

4. Apparatus according to claim 2 or 3, comprising a register file (8) characterized in that said register file (8) is extended with said FIFO register means (14).

25 5. Apparatus according to any one of claims 2 to 4, characterized in that said FIFO register (14) means comprises a plurality of FIFO registers.

6. Apparatus according to at least one of the preceding claims, characterized in that each of said functional units (10) are provided with at least one control unit (12).
7. Apparatus according to at least one of the preceding claims, which apparatus is adapted to execute a pipeline consisting of a plurality of stages, wherein each stage is executed by a functional unit (10).
8. Apparatus according to at least one of the preceding claims, characterized in that for each control unit (12) an instruction register and a counter are provided, wherein said counter indicates the number of times an instruction stored in said instruction register has to be executed by the corresponding functional unit (10).
9. Apparatus according to at least any one of the proceeding claims, further comprising a program memory means (6) storing a main program, characterized in that said main program contains directives for instructing said control units.
10. A method for processing digital signals in a digital signal processing apparatus, comprising a plurality of functional units (10) wherein each functional unit (10) is adapted to execute operations,
11. Method according to claim 9, characterized in that data-flow communication among said functional units (10) is supported by FIFO (first-in/first-out) register means (14).
12. A method for processing digital signals in a digital signal processing apparatus, comprising a plurality of functional units (10) wherein each functional unit (10) is adapted to execute operations,
- characterized in that data-flow communication among said functional units (10) is supported by FIFO (first-in/first-out) register means (14).

13. Method according to claim 11 or 12, wherein a pipeline consisting of a plurality of stages is provided, and each stage is executed by a functional unit (10).
14. Method according to at least any one of the claims 10 to 13, characterized in that the number of times an instruction stored has to be executed by a functional unit (10) is counted by the corresponding control unit (12).
15. Method according to at least any one of the claims 9 to 14, wherein a main program is stored in a program memory means (6),
- 10 characterized in that said main program contains directives for instructing said control units.